Claims 24-39 were rejected under 35 U.S.C. Section 102(b) as allegedly being "anticipated" by Nishiumi *et al.* (U.S. Patent No. 6,200,253). While not acquiescing in this rejection nor in the characterization of the reference made in connection therewith, claims 24, 30 and 36 have been amended. As such, Nishiumi *et al.* is discussed below with reference to the amended claims.

Nishiumi *et al.* discloses a controller control circuit 17 for receiving or transmitting data in a bit-serial fashion between bus control circuit 12 and connectors 181-184 to which game controllers may be connected. Claim 24 describes a video game system including an interface between connectors connectable to game controllers and a game program executing system. The interface comprises a double buffered output register and a double buffered input register corresponding to each connector. Nishiumi *et al.* shows a transmission circuit 172 and a reception circuit 173 connected to a RAM 174, but does not show double buffers arranged as claimed. Thus, Nishiumi *et al.* cannot anticipate claim 24 or its dependent claims 25-29.

Claim 30 describes a video game system including an interface between controllers and a game program executing system. The interface comprises first and second different storage devices for storing data transferred between the game program executing system and the controllers, and selector circuitry for selectively connecting the controllers to either the first and second storage devices. As shown in Figure 6, Nishiumi *et al.* includes a RAM 174 having storage areas 174a-174h for storing data. Nishiumi *et al.* does not disclose the claimed first and second different storage devices for data transferred between the game program executing system and the controllers, nor does

Nishiumi *et al.* disclose selector circuitry for selectively connecting the controllers to either one of such storage devices. Accordingly, Nishiumi *et al.* cannot anticipate claim 30 or its dependent claims 31-35.

Claim 36 describes a method of supplying data to a game program executing system in which received data is supplied from selector circuitry to a first storage device accessible by the game program executing system if the selector circuitry is in a first state and the received data is supplied from the selector circuitry to a different second storage device accessible by the game program executing system if the selector circuitry is in a second state. Nishiumi *et al.* discloses storing reception data in a RAM 174. Nishiumi *et al.* does not disclose using selector circuitry to supply received data to either a first storage device or a different, second storage device as claimed. Thus Nishiumi *et al.* cannot anticipate claim 36 or its dependent claim 37.

Claim 38 describes a method of supplying data from a game program executing system in which data from the game program executing system is selectively stored in first and second different storage devices connected to selector circuitry; stored data from the first storage device is supplied to the controllers if the selector circuitry is in a first state; and stored data from the second storage device is supplied to the controllers if the selector circuitry is in a second state. Nishiumi *et al.* discloses storing transmission data in RAM 174. Nishiumi *et al.* does not disclose using selector circuitry to supply data to controllers from either a first storage device or a different, second storage device as claimed. Thus, Nishiumi *et al.* cannot anticipate claim 38 or its dependent claim 39.

Claims 2-7, 14-18 and 21-23 were rejected under 35 U.S.C. Section 103(a) as allegedly being "obvious" over Scott-Jackson *et al.* (U.S. Patent No. 5,714,981) in view of Nishiumi *et al.* While not acquiescing in this rejection nor in the characterizations of the references made in connection therewith, claims 14 and 21 have been amended. As such, the references are discussed below with reference to the amended claims.

Claim 14 calls for a status register comprising one or more bits indicative of a status of a copy operation for copying data from one buffer to another of a double buffer. While Applicants do not agree, even if the temporary buffer and latch buffer of Scott-Jackson are viewed as a double buffer, there is no disclosure in Scott-Jackson of any registers which indicate the status of a copy operation for copying data from one of these buffers to the other. Nishiumi *et al.* likewise fails to disclose such a register. Thus, even assuming for the sake of argument that these references were properly combinable and that the combination were made, the subject matter of claims 14 and its dependent claims would not have resulted.

Claim 21 describes an interface for a video game system which includes a communication memory for storing variable size data, a double buffer for storing fixed size data and a switching device for selectively connecting either the double buffer or the communication memory to the controller. Neither Scott-Jackson nor Nishiumi *et al.* disclose or suggest such an interface nor would any combination of these references have fairly suggested the particular arrangement of a double buffer and a communication memory for different types of data as specified in claim 21. Accordingly, claim 21 and

its dependent claims would not have been obvious in view of Scott-Jackson and Nishiumi *et al.*

Claims 8-12 were rejected under 35 U.S.C. Section 103(a) as allegedly being "obvious" over the proposed Scott-Jackson-Nishiumi *et al.* combination, in further view of Takeda *et al.* The office action alleges that Takeda *et al.* discloses the error data of claims 8-12 and that it would have been obvious to provide such error data in the proposed Scott-Jackson-Nishiumi *et al.* combination. However, Takeda *et al.* does not remedy the deficiencies of the proposed Scott-Jackson-Nishiumi *et al.* combination with respect to claim 14, from which claims 8-12 depend. As such, even assuming for the sake of argument that Takeda *et al.* disclosed the claimed error data and that motivation could be found for combining Scott-Jackson, Nishiumi *et al.*, and Takeda *et al.*, the subject matter of claims 8-12 would not result from the combination.

New claims 40-47 have been added for the Examiner's consideration. The subject matter of these new claims is fully supported by the original disclosure and no new matter is added. New claims 40-43 each depends from one of claims 14, 21 and 24 and are believed to be allowable by virtue of this dependency and by virtue of reciting features not taught or suggested by the applied art. New claims 44 and 45 are directed to a video game system including a double buffered input register and a double buffered output register, wherein output data from the game program executing system is copied from a first output register to a second output register of the double buffered output register after the output data is written to the first output register, and copying from the first output register to the second output register is selectively lockable. In addition, input

data from the peripheral device is copied from a first input register to a second input register of the double buffered input register after the input data is written to the second input register, and copying from the first input register to the second input register is selectively lockable. Applicants respectfully submit that this arrangement is not taught or suggested by the applied art. New claims 46 and 47 are directed to a video game system including an interface which comprises a first storage device for storing data of a first type which is transmitted to or received from a peripheral device; a different, second storage device for storing data of a second type which is transmitted to or received from a peripheral device; and a switching device for selectively connecting the peripheral device to either the first storage device or the second storage device. Applicants respectfully submit that this arrangement is not taught or suggested by the applied art.

Applicants submit that the pending claims are allowable and early notice to that effect is respectfully requested.

Respectfully submitted,

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Version marked to show changes made

IN THE CLAIMS

Claims 14, 21, 24, 30, 36 and 39 have been amended as follows:

14. (Twice Amended) A video game system, comprising:

a game program executing system executing a game program;

one or more controllers supplying user inputs to the game program executing system;

an interface between the controllers and the game program executing system, the interface [system] being programmable to periodically poll the controllers without involvement of the game program executing system, wherein the interface comprises:

a double buffer for storing data transferred between the game program executing system and the controllers; and

[a communication RAM for storing data transferred between the game program executing system and the controllers]

a status register comprising one or more bits which are indicative of a status of a copy operation for copying data from one buffer to another of the double buffer.

21. (Twice Amended) A video game system, comprising:

a game program executing system executing a game program;

a controller supplying user inputs to the game program executing system; and

an interface interfacing between the game program executing system and the controller, the interface including communication circuitry operable in a first mode in which data of a fixed size is communicated between the game program executing system and the controller and in a second mode in which data of variable size is communicated between the game program executing system and the controller, wherein the interface further comprises:

a communication memory for storing the variable size data;[and]

a double buffer for storing the fixed size data; and

a switching device for selectively connecting either the double buffer or the communication memory to the controller.

24. (Amended) A video game system, comprising:

a game program executing system having connectors connectable to one or more game controllers; and

an interface between the connectors [game controllers] and the game program executing system, the interface comprising a double buffered input register and a double buffered output register corresponding to each connector, each double buffered output register comprising first and second output registers for storing data from the game

program executing system for output to a controller connected thereto and each double buffered input register comprising first and second input registers for storing data from a controller connected thereto for input to the game program executing system.

30. (Amended) A video game system, comprising:

a game program executing system supplied with user inputs from one or more game controllers; and

an interface between the controllers and the game program executing system, the interface comprising first and second different storage devices for storing data transferred between the game program executing system and the controllers, and selector circuitry for selectively connecting the controllers to either [selecting between] the first and second storage devices.

36. (Amended) A method of supplying data to a game program executing system of a video game system from controllers connected thereto, the method comprising:

receiving data from the controllers;

supplying the received data to selector circuitry;

supplying the received data from the selector circuitry to a first storage device accessible by the game program executing system if the selector circuitry is in a first state; and

supplying the received data from the selector circuitry to a different, second storage device accessible by the game program executing system if the selector circuitry is in a second state.

39. (Amended) The method according to claim 38, wherein fixed-size data from the game program executing system is stored in the first storage device and variable-size data from the game [fame] program executing system is stored in the second storage device.